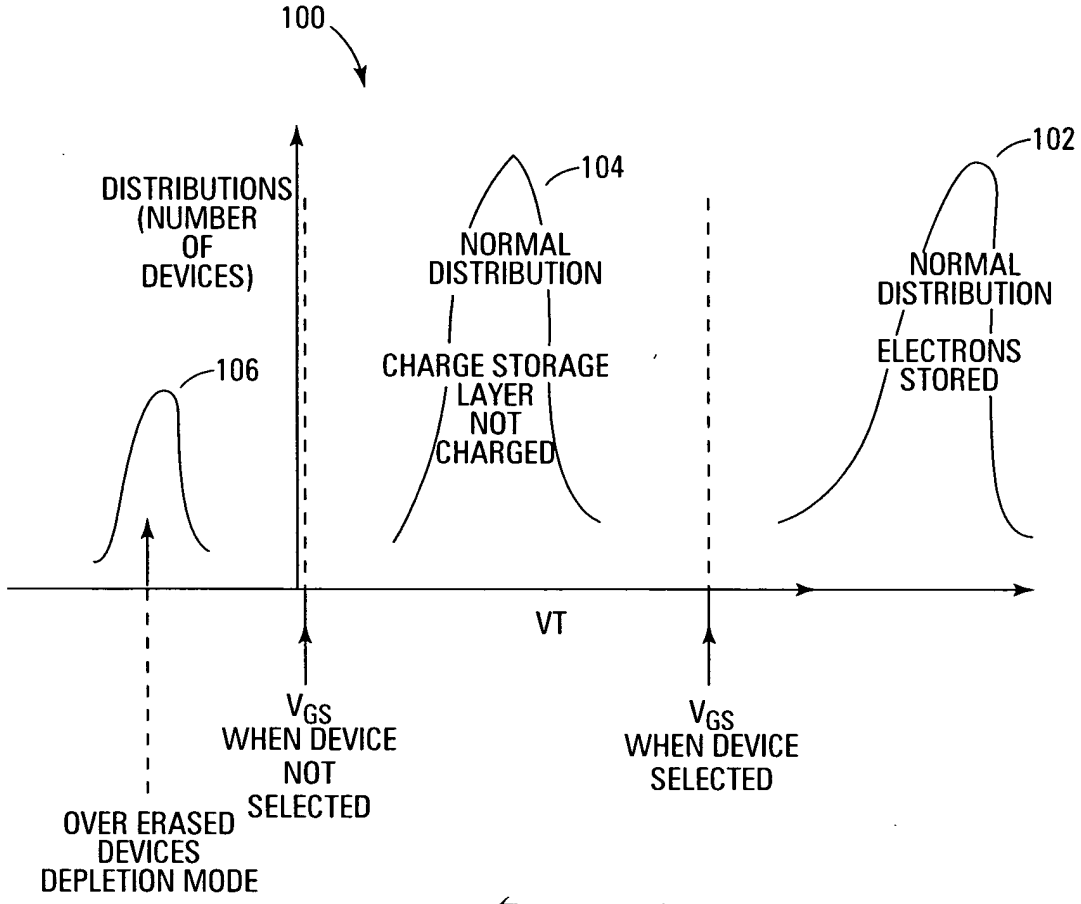

100
DISTRIBUTIONS (NUMBER OF DEVICES)
104
NORMAL DISTRIBUTION
CHARGE STORAGE LAYER NOT CHARGED
102
NORMAL DISTRIBUTION
ELECTRONS STORED
106
VT
V_{GS} WHEN DEVICE NOT SELECTED
V_{GS} WHEN DEVICE SELECTED
OVER ERASED DEVICES DEPLETION MODE

Fig. 1A

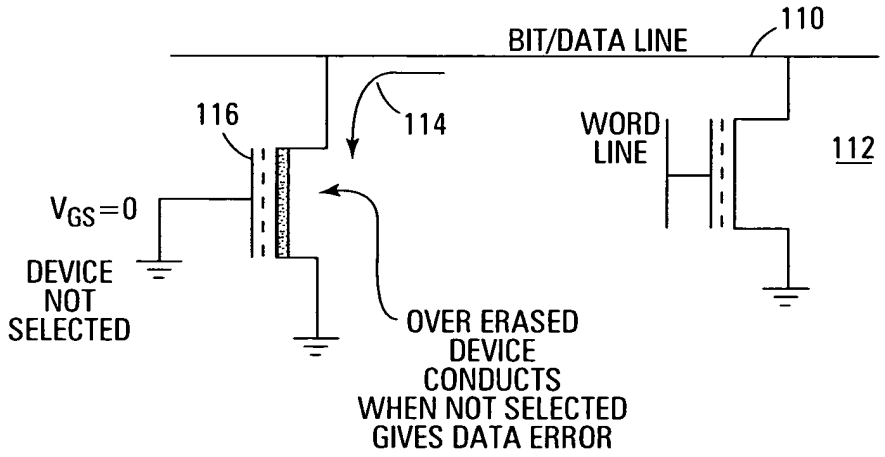

BIT/DATA LINE
110
116
114
WORD LINE
112
$V_{GS}=0$
DEVICE NOT SELECTED
OVER ERASED DEVICE CONDUCTS WHEN NOT SELECTED GIVES DATA ERROR

Fig. 1B

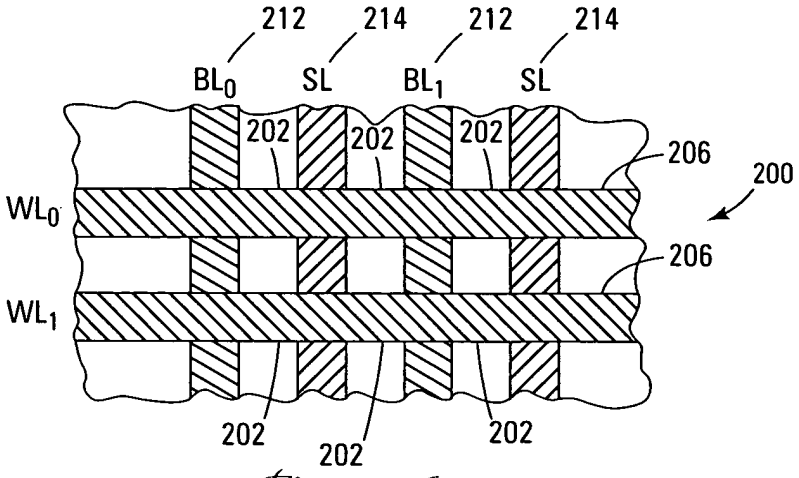


Fig. 2A
Prior Art

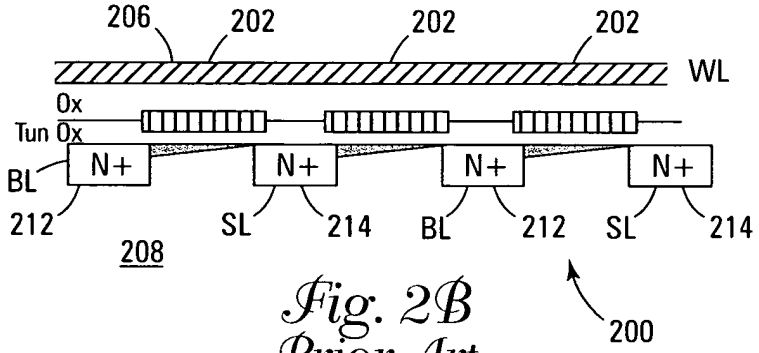


Fig. 2B
Prior Art

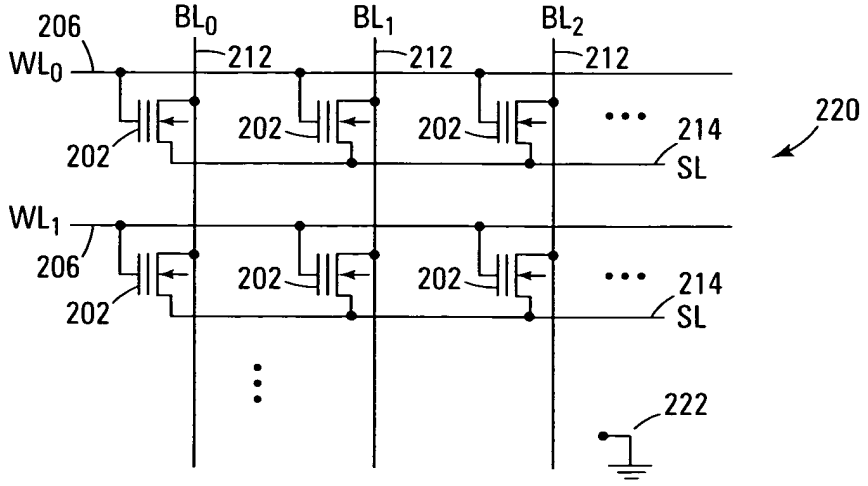


Fig. 2C
Prior Art

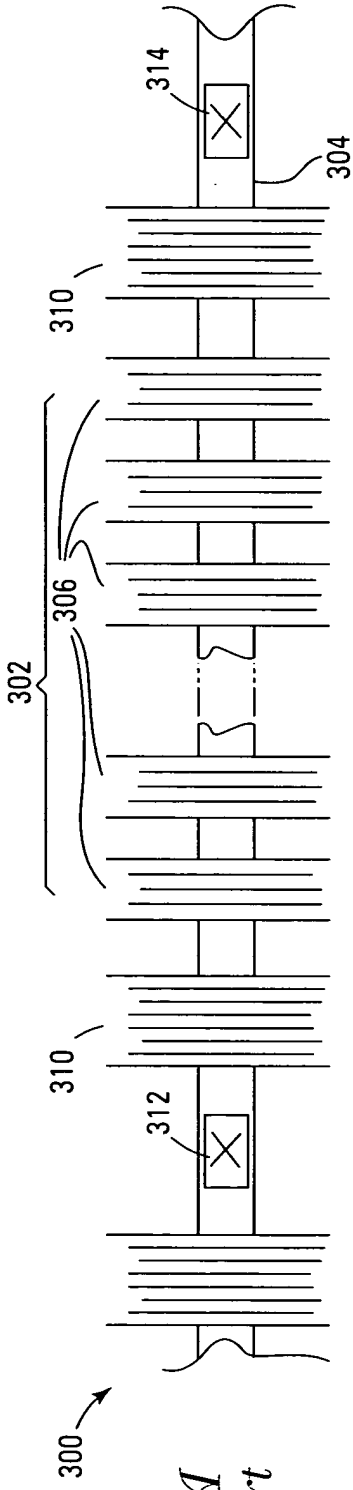


Fig. 3A
Prior Art

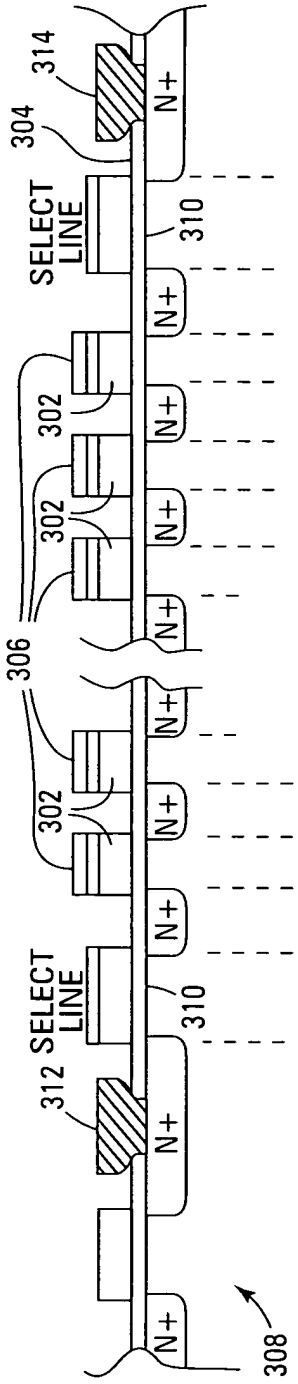


Fig. 3B
Prior Art

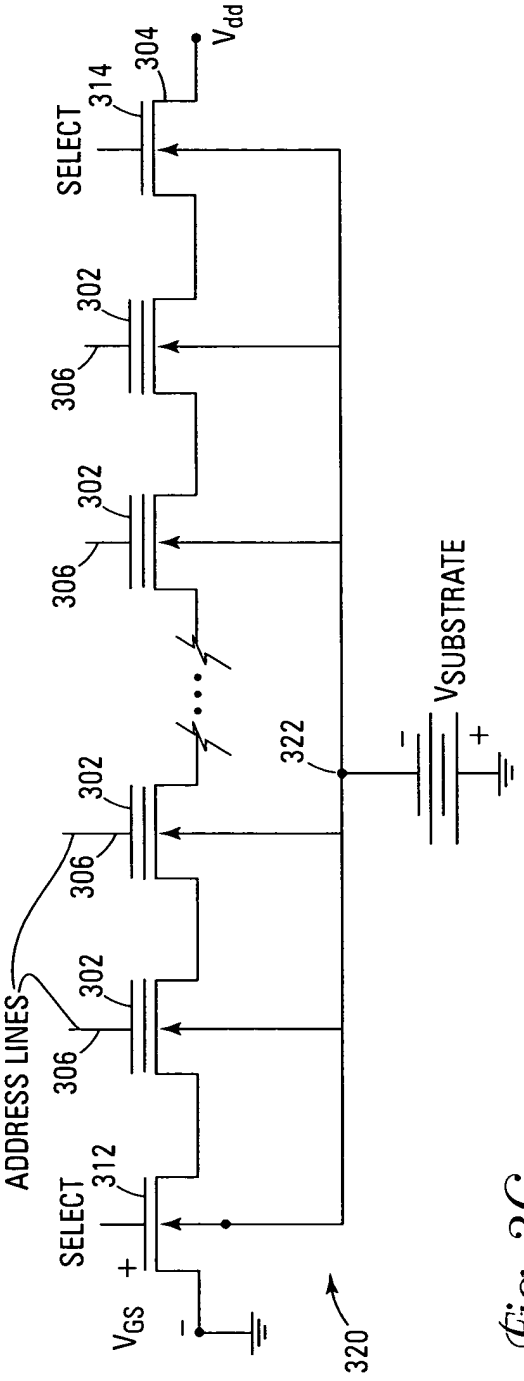


Fig. 3C
Prior Art

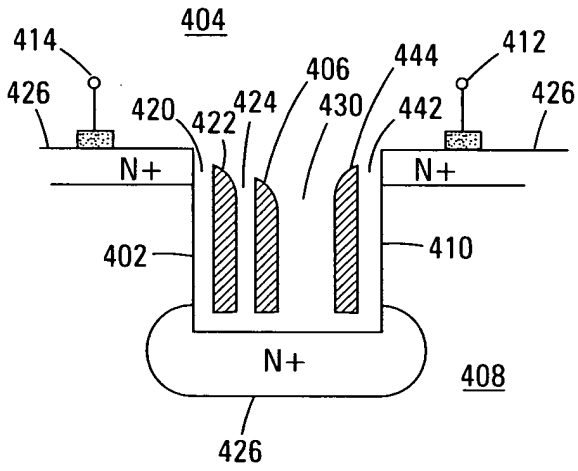

404
414
412
426
420
422
424
406
444
430
442
426
N+
N+
402
410
N+
408
426

Fig. 4A

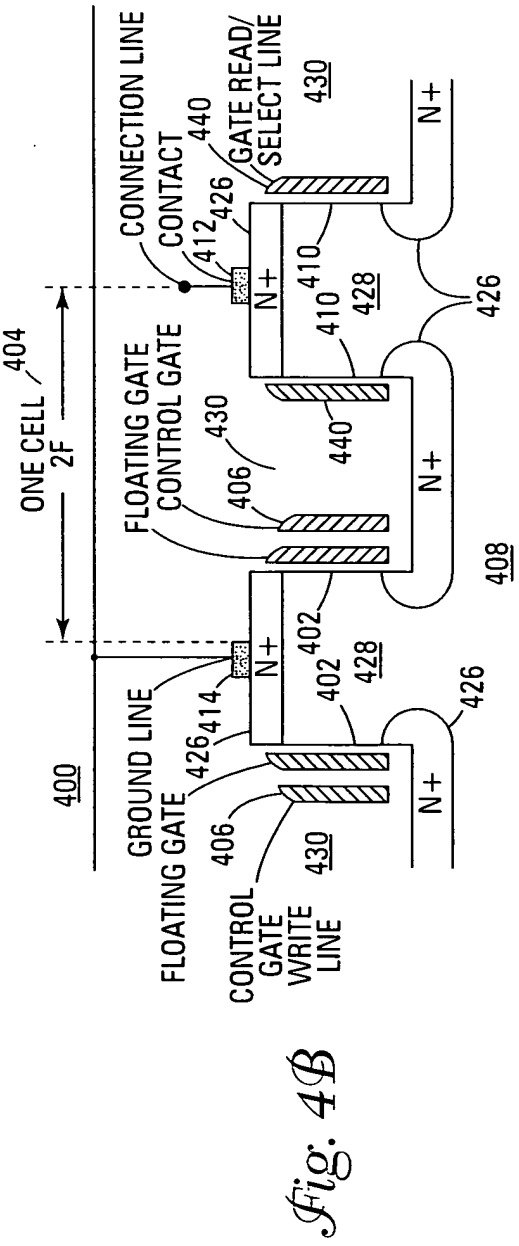

ONE CELL
2F
404
400
GROUND LINE
FLOATING GATE
CONTROL GATE
CONTROL GATE WRITE LINE
CONNECTION LINE
CONTACT
GATE READ/ SELECT LINE
N+
406
410
412
414
426
428
430
440
402
408

Fig. 4B

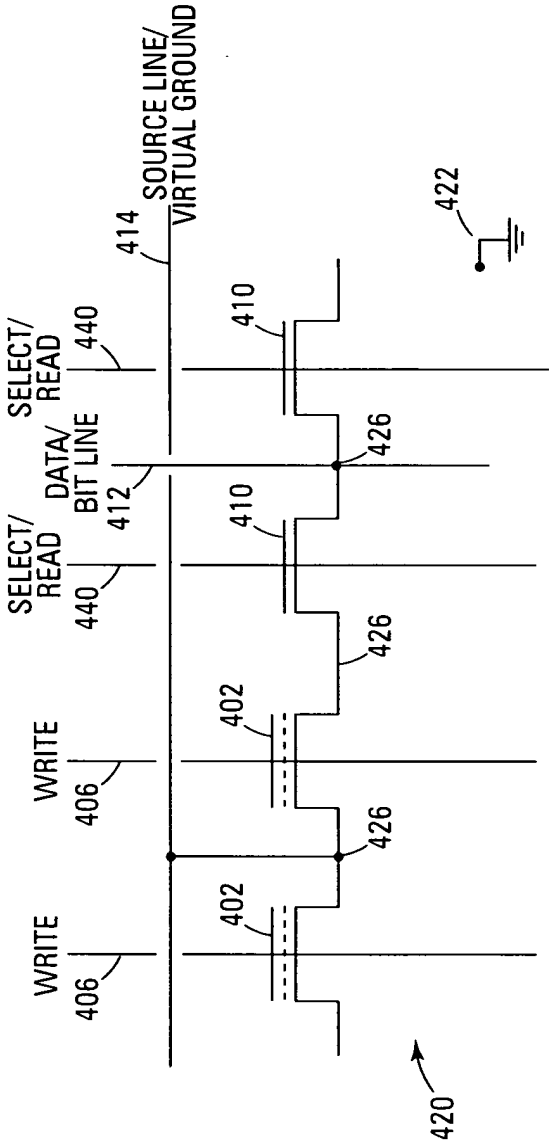

SOURCE LINE/ VIRTUAL GROUND
SELECT/ READ
DATA/ BIT LINE
WRITE
406
410
412
414
422
426
440
402
420

Fig. 4C

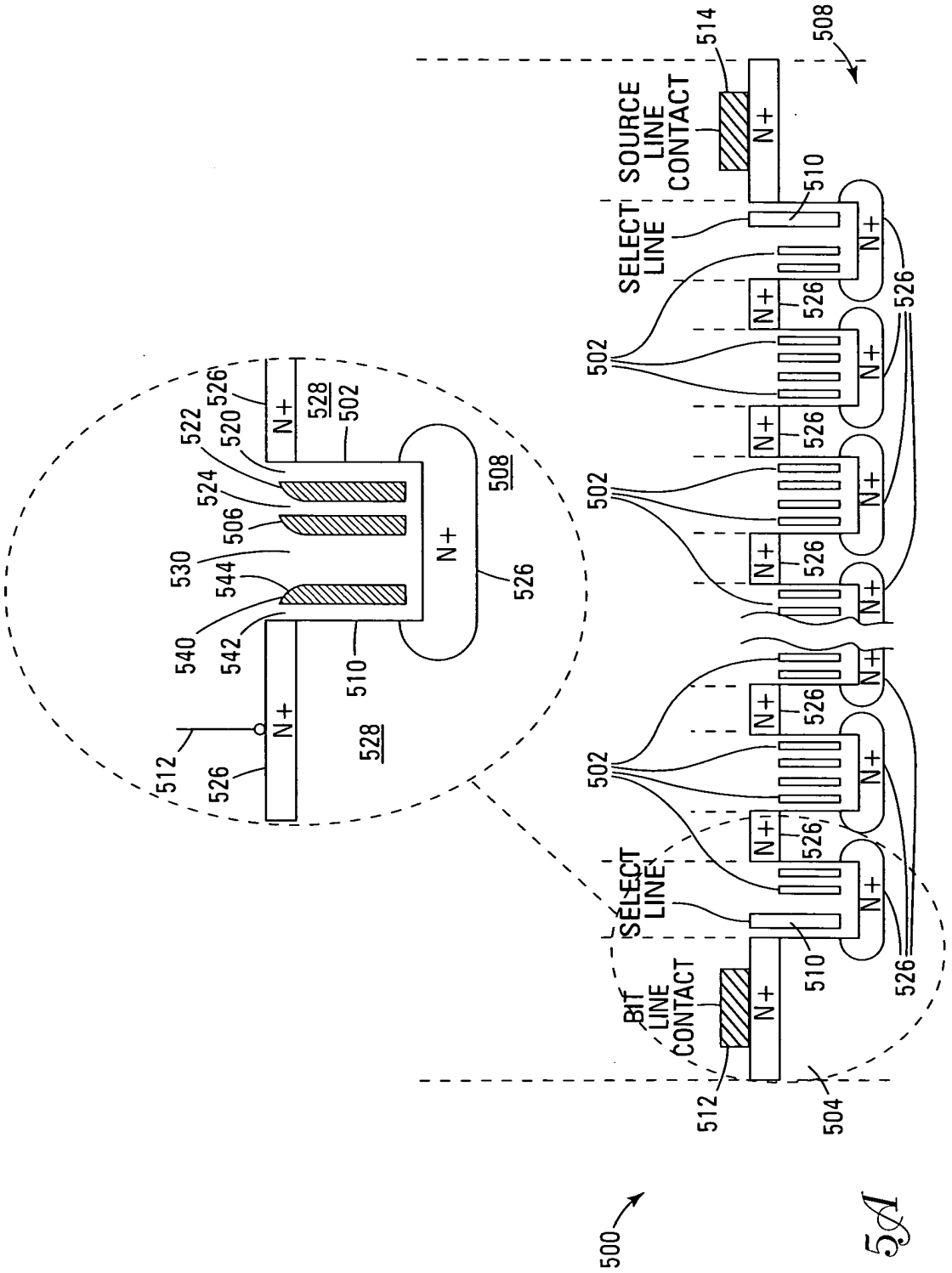

500
502
504
506
508
510
512
514
520
522
524
526
528
530
540
542
544
N+
SOURCE LINE CONTACT
SELECT LINE
SELECT LINE
BIT LINE CONTACT

Fig. 5A

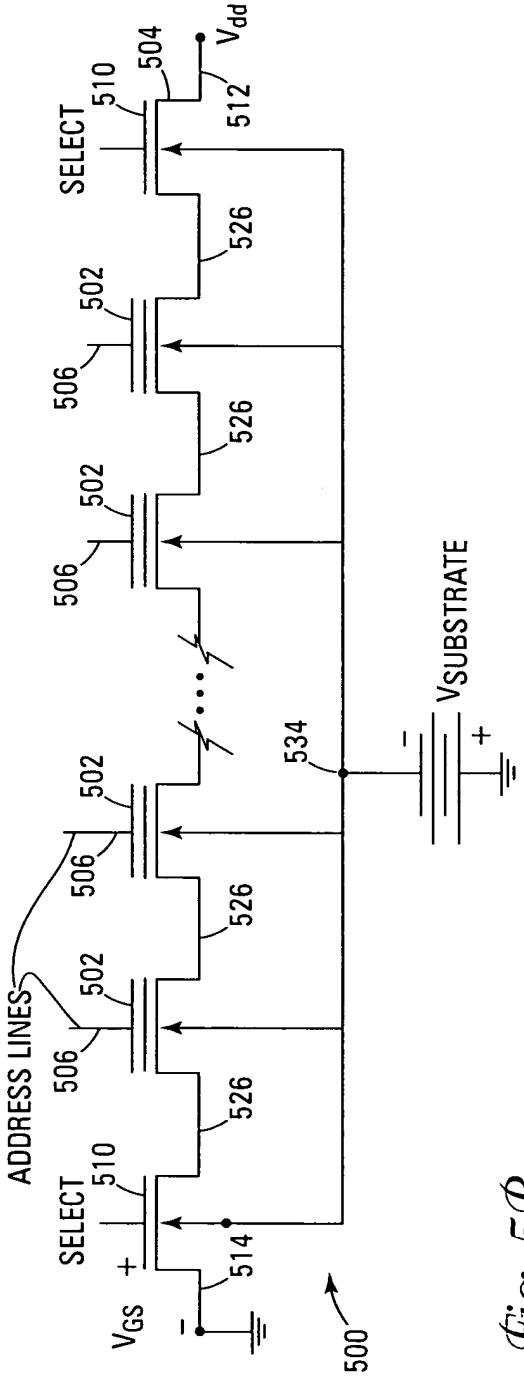

SELECT
510
504
V_{dd}
512
526
502
506
526
502
506
526
502
506
526
502
506
ADDRESS LINES
526
SELECT
510
514
V_{GS}
534
$V_{SUBSTRATE}$
500

Fig. 5B

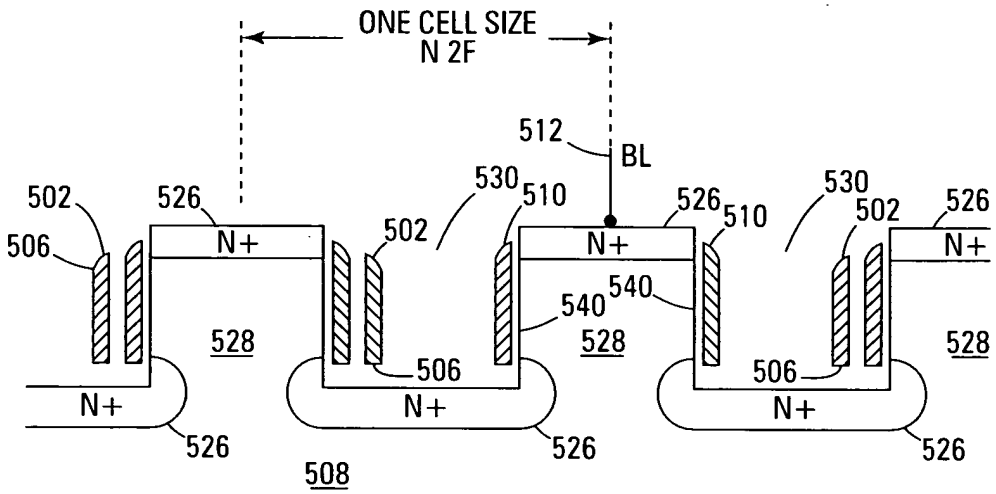

ONE CELL SIZE
N 2F
512
BL
502
526
530
510
506
N+
528
540
508

Fig. 5C

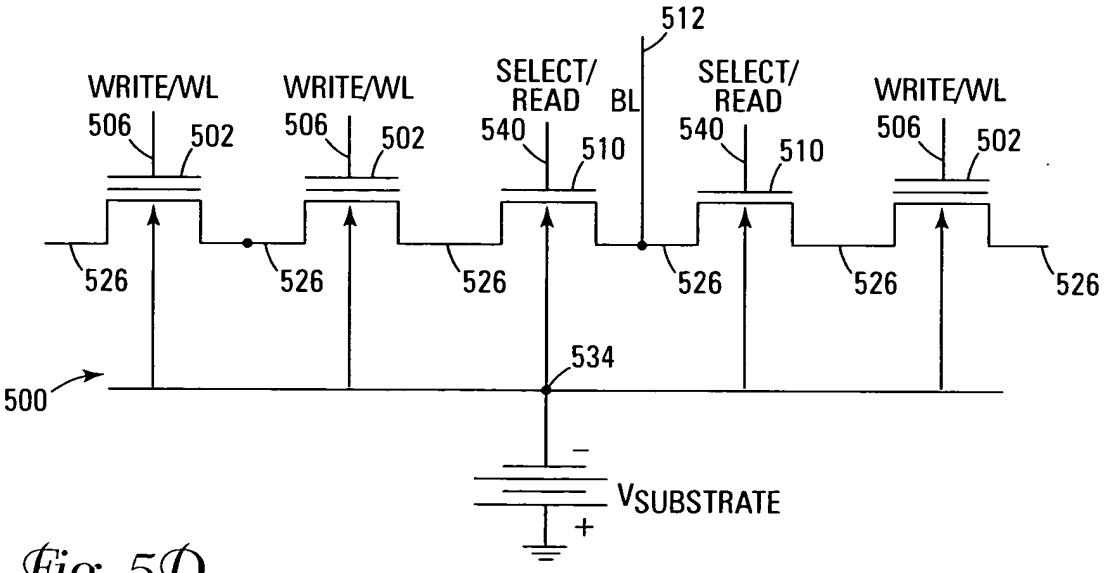

512
WRITE/WL
SELECT/
READ
BL
506
502
540
510
526
534
500
VSUBSTRATE
+
−

Fig. 5D

Fig. 6A

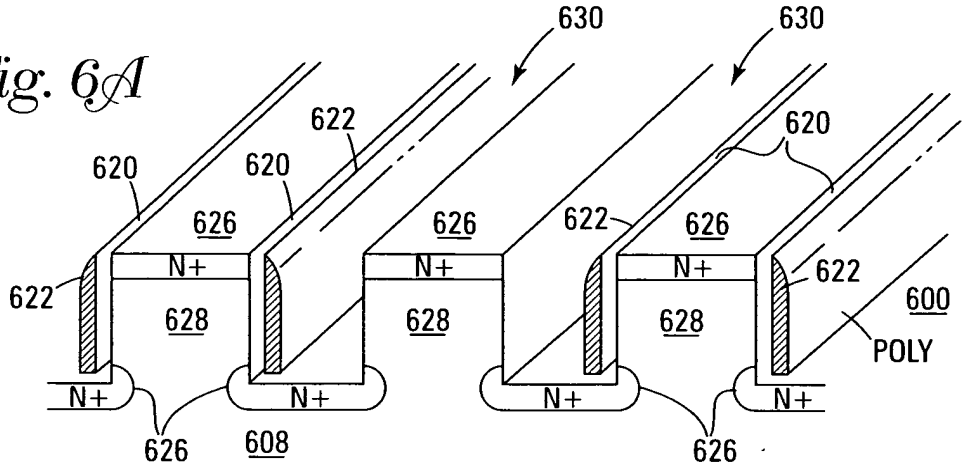


Fig. 6B

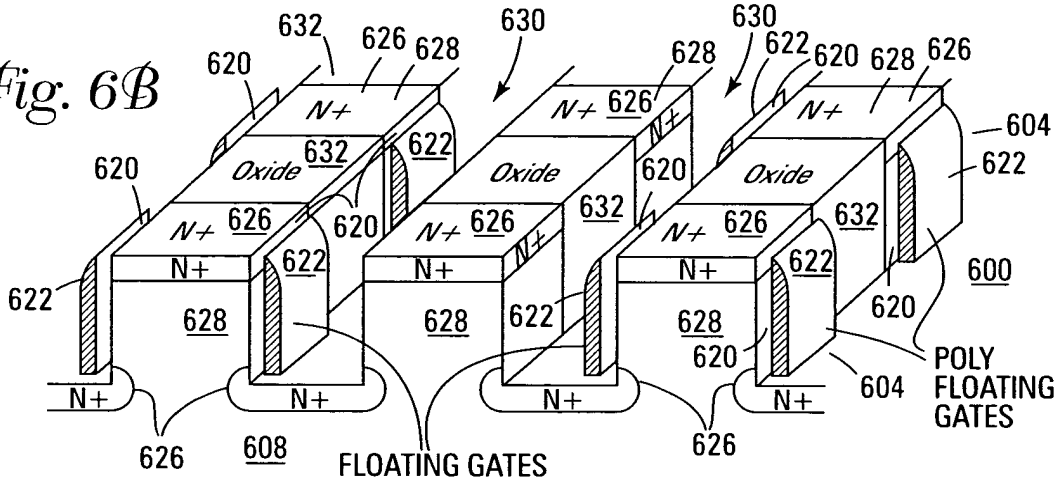
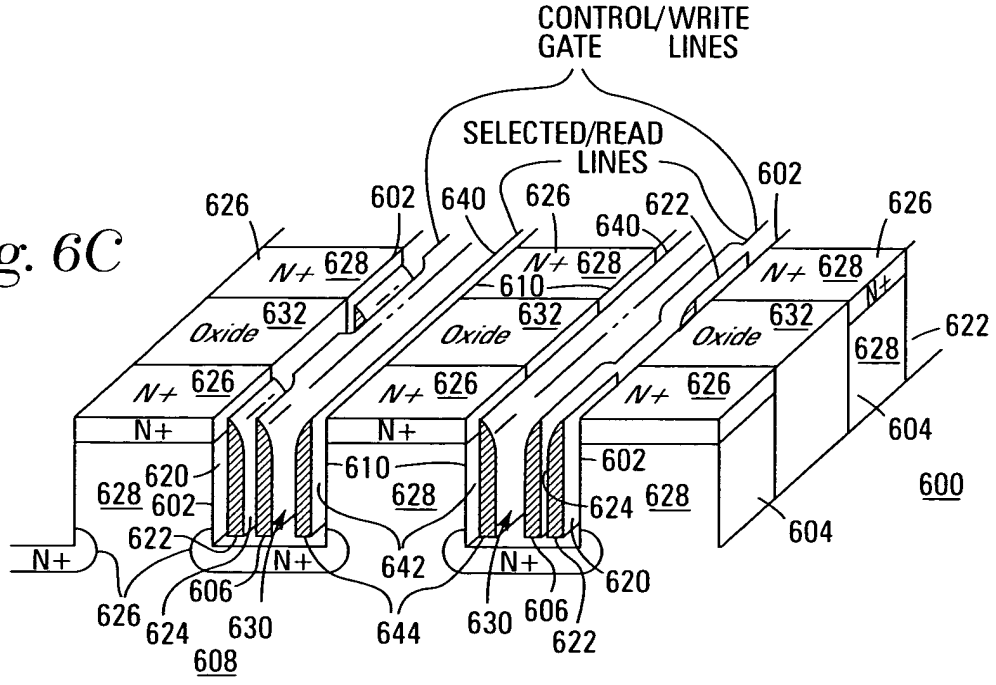


Fig. 6C



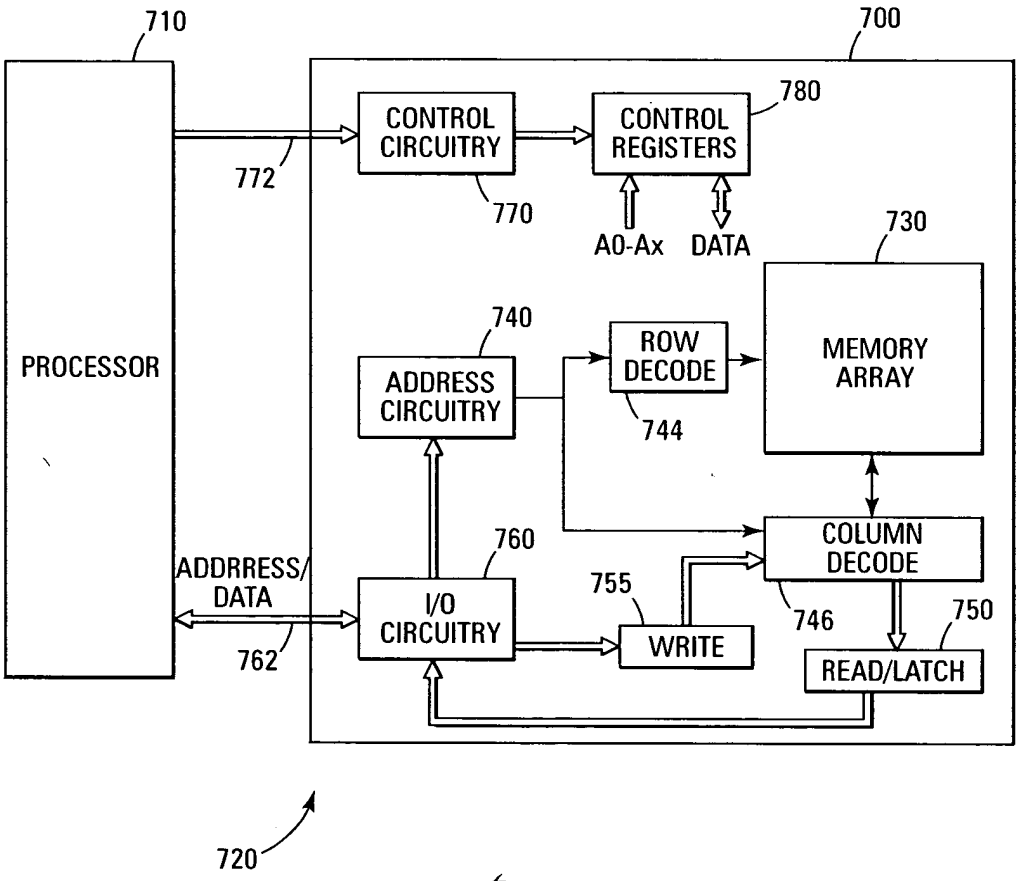

710
700
PROCESSOR
CONTROL CIRCUITRY
CONTROL REGISTERS
780
772
770
A0-Ax
DATA
730
740
ADDRESS CIRCUITRY
ROW DECODE
MEMORY ARRAY
744
COLUMN DECODE
760
ADDRRESS/ DATA
I/O CIRCUITRY
755
WRITE
746
750
READ/LATCH
762
720

Fig. 7